**DC-DC CLLLC Resonator Software design Document**

# Plant model

The overview of the DC-DC CLLLC Resonant converter consists of an input inverter to convert the input DC voltage to AC voltage, an input Capacitor and Inductor tank connected in series, a Transformer with a magnetizing inductance, an Inductor and Capacitor tank connected in series, a current controlled rectifier bridge for synchronous rectification and an output capacitor The system also consists of input voltage sensing, input current sensing, Primary side resonant Tank current sensing, Secondary side resonant Tank current sensing, Load/output current sensing, output voltage sensing, a MCU for control, and gate drivers to drive the FETs. The chosen MCU for the application is the Texas instruments [F28069m](https://www.ti.com/tool/LAUNCHXL-F28069M?utm_source=google&utm_medium=cpc&utm_campaign=epd-c2x-null-prodfolderdynamic-cpc-pf-google-wwe&utm_content=prodfolddynamic&ds_k=DYNAMIC+SEARCH+ADS&DCM=yes&gclid=Cj0KCQjw3v6SBhCsARIsACyrRAklrhDMmNKasowDrrIfKbNlJ5QYCcJ0WlZR8FNb1obrrISz5O3HVjYaAve4EALw_wcB&gclsrc=aw.ds) launch pad. The CLLLC converter receives its input voltage from the PFC power factor correction AC-DC convert

Diagram

Description automatically generated

Figure 1.1: System overview showing Resonant Converter architecture, MCU, gate driver, FETs, current and voltage sense

## switching model SIMULINK

Below is a simplified switching model of the CLLC, the Converter functions by switching the leading and Lagging MOSFET with complementary duty cycles being driven at 50 percent, energy flow through the inverter (H-bridge on the right of the picture and subsequently the resonant Tank is modulated by PFM(pulse frequency modulation), with the maximum energy flow occurring near the resonant frequency of the Tank and the minimum occurring at much larger frequencies.

Diagram

Description automatically generated

Figure 1.2: simplified model of a single-phase PFC showing the configuration of the inductor, high frequency switches, rectification diodes and output capacitance

## transfer function

### Inner Current loop Transfer function

The open- loop plant transfer function generated from Simulink system Identification tool box by building an electrical system model of the converter using Simscape electrical and extracting the input output data, which corresponds to the input frequency and output current respectively. The 2nd order system approximation of the transfer function in the frequency domain has a 20db DC gain, cross over frequency 1 Kkz, and phase margin of 90 degrees

Text, letter

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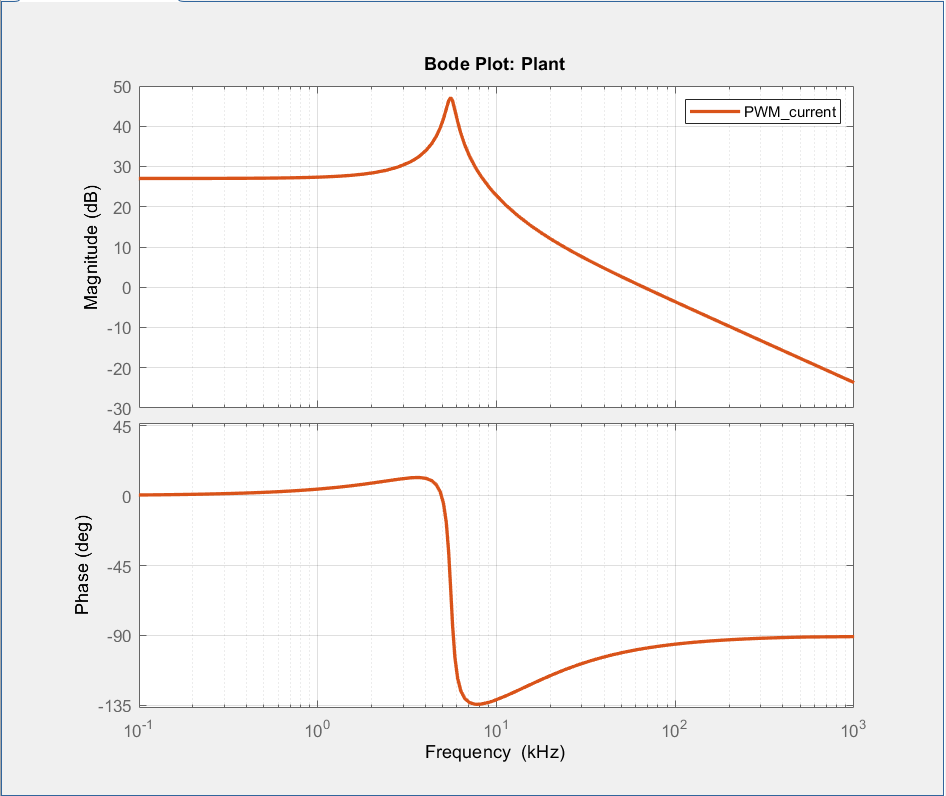
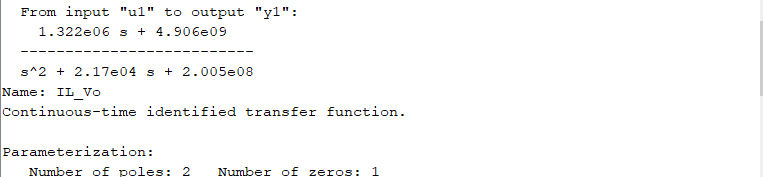


Figure 1.3: Bode plot of the open loop plant Transfer with input duty cycle and output current.

### Outer Voltage loop Transfer function

The Input output data, which corresponds to the input current and output voltage respectively is also used to generate a Voltage transfer function. The 2nd order system approximation of the transfer function in the frequency domain has a 20db DC gain, cross over frequency 1 Kkz, and phase margin of 90 degrees



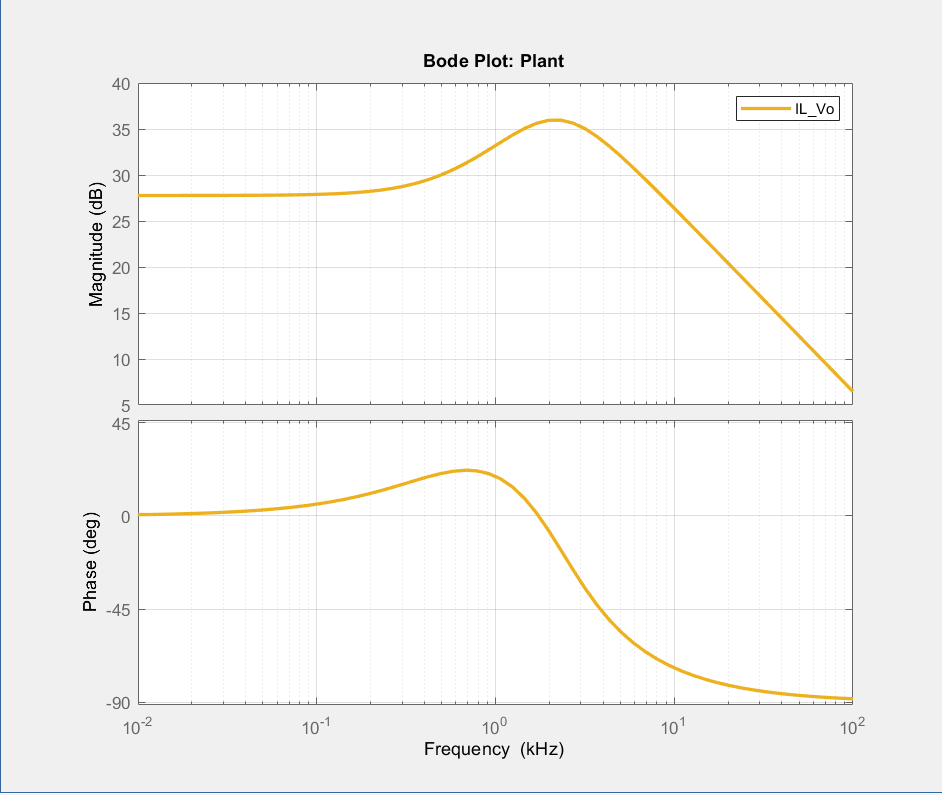


Fig 1.4 :Bode plot of the open loop plant Transfer with input current and output voltage.

# Closed loop current Controller

## Current control Architechture

PI Controller

Current reference

error

PWM Timer period/Frequency modulation

Current feedback

Figure 2.1: Control loop for current controller

Chart

Description automatically generated

Step response of the closed loop controller

## PI Controller gain

Proportional gain: 0.027

Integral gain: 140

## Feedback gains

Current Sensor gain:

ADC gain :

# Closed loop Voltage controller

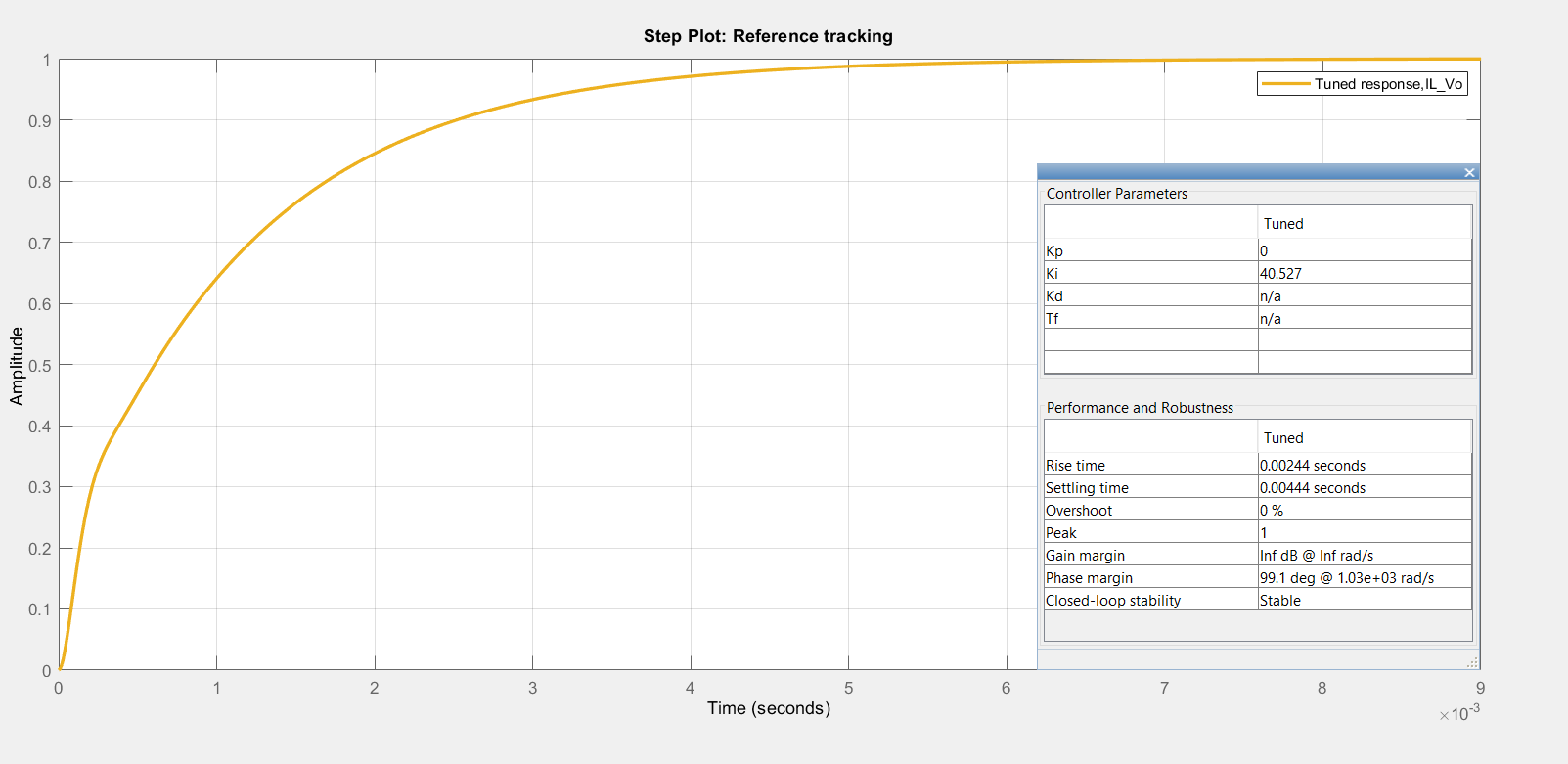
## Voltage control Arcitechture

PI Controller

Voltage reference error signal Inductor current reference

Voltage feedback

Figure 3.1: Control loop for voltage controller



## Controller gains

Proportional control gain: 0.03

Integral Controller gain: 0.4

## Feedback gains

Voltage sensor gain

ADC gain:

# Filters

## 20Khz lowpass filter for CURRENT measurment

Low pass filter to remove high frequency switching noise: design second order low pass filter with cut-off frequency at 50 khz

Figure 5.1: 20 khz generated low pass filter frequency response

## 1khz low pass filter for voltage measurment

Low pass filter to remove high frequency noise above 10 Khz

Graphical user interface

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Figure 5.2: 1 khz hz generated low pass filter frequency response

## 500Hz low pass filter for Temperature measurment

Low pass filter 1kz to remove noise low pass filter to noise

Fig 5.3: Frequency response of second order low pass filter 1khz

# Peripheral setup

## Pin Mapping

|  |  |  |
| --- | --- | --- |
| Signal | GPIO designation | Hardware peripheral |
| **primary side gate driver** |  |  |
| Highside switch 1A Pri | P0 | EPWM 1A |
| Lowside switch 1B Pri | P1 | EPWM 1B |
| Highside switch 2A Pri | P2 | EPWM 2A |
| Lowside switch 2B Pri | P3 | EPWM 2B |
| **Secondary side gate driver** |  |  |
| highside switch 3A sec | P4 | EPWM 3A |
| lowside switch 3B sec | P5 | EPWM 3B |
| highside switch 4A sec | P6 | EPWM 3A |
| lowside switch 4B sec | p7 | EPWM 3B |
|  |  |  |
| **GPIO** |  |  |
| Vin Control Signal | p13 |  |
| input Voltage indication | p50 |  |
| Primary HVDC Input fault | p51 |  |
| Primary HVDC input indication | p55 |  |
| secondary HVDC output fault | P27 |  |
| secondary HVDC output indication | p26 |  |
|  |  |  |
|  |  |  |
| **Voltage sensing** |  |  |
| Sec Voltage\_ADC |  | AA0 |
| Prim \_Voltage\_ADC |  | AA1 |
|  |  |  |
| **Current sensing and reference** |  |  |
| Sec Current\_ADC |  | AA4 |
| Prim Current\_ADC |  | AA3 |
| Resonant Tank Prim Current \_ADC |  | AA6 |
| Resonant Tak Sec Current\_ADC |  | AB0 |
| sec current zero volt ref\_ADC |  | AA5 |
| Resonant Tank Prim current zero volt ref\_ADC |  | AA7 |
| Rosonant Tank secondary current zero volt\_ref\_ADC |  | AB1 |
| prim current zero volt REF\_ADC |  | AA2 |
|  |  |  |
| **Temperature sensing** |  |  |
| Tempsensing 1 ADC |  | AB2 |
| Temp Sensing 2\_ADC |  | AB3 |
| Temp Sensing 3\_ADC |  | AB4 |

## PWM

### Inverter bridge

#### Counting mode

Up down counter

#### operating frequency

Operating frequency of the CLLLC converter (resonator) ranges from the tank resonant frequency 65000 Khz to 300000 khz, which corresponds to a PWM period length of 151 to 900 respectively

#### Duty Cycle

The duty cycle of the PWM is a constant 50 percent of the duty counter period and is gotten from dividing the control input; counter period into two and feeding as the counter compare variable used in setting duty cycle.

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Fig 6.1: configuration of PWM frequency, mode and Duty cycle

#### dead band

The dead band between the high side and low side switch needs to be 10 clock cycles with the RED applied to the ePWMA and FED applied to ePWMB

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Fig 6.2: configuration of PWM with Deadband

#### ADC event trigger

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Fig 6.3: configuration of PWM for ADC trigger used in measuring current

### Rectifier Frequency bridge

#### Operating frequency

N/A

#### Counting mode

Up-down count

#### Duty Cycle

899 or 100%

#### PHASE shift

N/A

#### Dead band

10 clock cycles

## ADC (Analog to digital converter)

### Output DC bus voltage

Software Triggered measurement sampled at 1khz with variable TS\_Voltage

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Fig 6.4 configuration output DC bus voltage measurment ADC

### Input dc current

PWM triggered measurement at 100khz sampled at the middle of the PWM counter by ePWM4

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Fig 6.5(a & b) configuration of ADC measurement and reference for input current

### Output dc current

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Fig 6.6(a & b) configuration of ADC measurement and reference for output current

### Input resonant tank current

sampled at 100khz measured at the middle of the PWM counter

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Description automatically generated

Fig 6.7(a & b) configuration of ADC measurement and reference for output current

### Output resonant tank current

sampled at 100khz measured at the middle of the PWM counter

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### Input DC bus voltage

Software triggered interrupt sampled at 1khz

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Fig 6.7a

# Software in the loop (sil)

The controller is simulated in Simulink with the plant model load at 50 ohms and the controller in continuous time

Fig 7.1 : result of the software in the loop solution showing PFC output voltage, inductor current, input voltage, and PI current controller output respectively.

# APPENDIX

## Abbreviations

PWM – pulse width modulation

ADC – analog to digital converter

kHz – kilo hertz

DC- direct current

AC- alternating current

CCM- continuous conduction mode

PFC – power factor correction

FET – field effect transistor

MCU -microcontroller unit

RED – rising edge dead band

FED – falling edge dead band